patterns are present, the additional designing time would be enormously large, which would increase the turnaround time, thus increasing the manufacturing cost.

Please replace the paragraph beginning at page 6, line 11, with the following rewritten paragraph:

A first embodiment of a method for manufacturing a semiconductor device consistent with the invention will be explained next with reference to Figs. 5A, 5B, 5C, 6A, 6B, 6C and 7.

Please replace the paragraph beginning at page 6, line 25, with the following rewritten paragraph:

Finally, referring to Fig. 5C, the active area patterns A1 and A2 and the dummy area patterns D are combined together to complete the first photomask M1.

Please replace the paragraph beginning at page 7, line 3, with the following rewritten paragraph:

Finally, referring to Fig. 6C, the gate patterns GP1 and GP2 and the dummy gate patterns DP are combined together to complete the second photomask M2.

Please replace the paragraph beginning at page 7, line 17, with the following rewritten paragraph:

The method for manufacturing the semiconductor device of Fig. 7 is explained next with reference to Figs. 8A through 8K, which are cross-sectional views taken along the lines X-X and Y-Y in Fig. 7.

Please replace the paragraph beginning at page 7, line 21, with the following rewritten paragraph:

First, referring to Fig. 8A, a monocrystalline silicon substrate 1 is thermally oxidized to form a silicon oxide layer 2 thereon. Then, a silicon nitride layer 3 is deposited on the silicon oxide layer 2. Then, a photoresist layer 4 is coated on the silicon nitride layer 3. Then, the

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a7

photoresist layer 4 is irradiated with ultraviolet light via the photomask M1 of Fig. 5C. Then, the photoresist layer 4 is developed, so that the photoresist layer 4 is patterned.

Please replace the paragraph beginning at page 7, line 29, with the following rewritten paragraph:

Next, referring to Fig. 8B, the silicon nitride layer 3 is etched by using the photoresist layer 4 as a mask and the silicon oxide layer 2 as an etching stop. Then the silicon oxide layer 2 is etched by using the silicon nitride layer 3 as a mask. Then, the photoresist layer 4 is removed.

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Please replace the paragraph beginning at page 8, line 6, with the following rewritten paragraph:

Next, referring to Fig. 8E, a CMP process is carried out to flatten the silicon oxide layer 6 using the silicon nitride layer 3 as a stop.

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IN THE CLAIMS:

Kindly cancel claims 12-32, without prejudice.

Please add new claims 33-36 reading as follows:

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--33. A method for manufacturing a semiconductor device, comprising the steps of:

forming a shallow trench isolation layer in a semiconductor substrate, so that active areas and a field area including dummy areas for isolating said active areas are partitioned; and

forming gates on said active areas and dummy gates on said dummy areas;

wherein the shape of at least one said dummy area and/or dummy gate is a polygon other than a square or a rectangle.

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